

CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

- 1 1. A method of forming a raised source/drain field effect transistor including the steps
 2 of:
 3 etching a gate region sufficient for silicidation of contacts in a substrate;
 4 forming a gate structure at said gate region;
 5 growing boron doped amorphous silicon on NFET and PFET regions, adjacent
 6 said gate region, by selective epitaxy;
 7 forming an abrupt source/drain junction for PFET boron extension electrode
 8 and NFET boron halo formation adjacent said gate region; and
 9 etching dual spacers in said source/drain junction.
- 1 2. The method of claim 2, further comprising the steps of:
 2 performing N-extension arsenic implantation and P-extension boron
 3 implantation; and
 4 diffusing said arsenic and said boron such that said PFET extension electrode
 5 overlaps the gate region.
- 1 3. The method of claim 2, where the N-extension arsenic does not substantially
 2 overlap the gate region.
- 1 4. The method of claim 1, further comprising the step of performing selective
 2 amorphous growth to form the source/drain junction.

1 7. The CMOS Structure of claim 6, where the N-extension arsenic does not
2 substantially overlap the gate region.